SPECIFICATION AMENDMENTS:

Please amend the paragraph beginning at page 4, lines 3 and 4 as follows:

"FIG. 1 is a diagram illustration of beamforming~~, in accordance with the present invention~~ as known in the art;"

Please amend the paragraph beginning at page 4, lines 5 and 6 as follows:

"FIG. 2 is a block diagram illustrating one embodiment of a circuit in accordance with ~~the FIG. 1~~ the present invention;"

Please amend the paragraph beginning at page 4, lines 7 and 8 as follows:

"~~IG. 3A-3C~~ FIGS. 3A and 3B are block diagrams illustrating alternative multipliers for the device of FIG. 2, and FIG. 3C is a variable shift unit as an alterative variable shift unit for the multiplier of FIG. 3B;"

Please amend the paragraph beginning at page 4, lines 7 and 8 as follows:

"FIG. 4 is an illustration of signal encoding, as required by the multipliers of FIG. ~~3A-3C~~ 3A and 3B; and"

Please amend the paragraph beginning at page 5, lines 11-27 as follows:

"FIG. 2 is a block diagram illustrating one embodiment of a beamforming circuit 200, in accordance with the invention. In one embodiment of the invention, the transmit circuit 220 and receive circuit 230, for a single piezoelectric transducer 215 combine to create a channel 210 of the beamforming circuit 200. The circuit 220 is one embodiment of a beamforming circuit that can be used for transmit beamforming on a single channel. A phase counter 205 may monotonically increase the phase used to reference a sinewave signal stored digitally in a look-up table (LUT) 207. A channel-specific delay (not shown) can be added 206 to the phase for the purpose of beamforming. The output of the LUT 207 may be turned into an analog signal by means of a digital-to-analog converter (DAC) 225. The signal may then be transmitted to the piezoelectric transducer 215 One embodiment of a complimentary

circuit to the beamforming transmit circuit 220 may be illustrated as a receive circuit 230. An embodiment of the invention may first digitize the signal 235 from the same transducer 215 when in the receive mode. The signal may then be delayed for focusing. A digital delay 250 can be implemented for one embodiment of the invention with a string of registers and a multiplexer, or with a FIFO logic implemented using a RAM. Delayed signals from all channels forming a transducer array may be summed together 270 via multipliers 260 to create a scan line."

Please amend the paragraph beginning at page 6, lines 21-27 as follows:

The multiplication operation can be simplified with respect to a [[full]] multiplier 301, as that shown in FIG. 3A. One method is the quantization of one operand to a small set of quantization levels. Constant values may lead to even more savings but in one embodiment of the invention, it may be assumed that both operands of the multiplier are time variant, or at least programmable. Different sets of quantization levels offer various cost and performance points. If the statistics of a signal are known, then quantization levels can be optimized for this particular signal."

Please amend the paragraph beginning at page 7, lines 1-8 as follows:

"A possible implementation of the multiplication operator is a floating-point multiplier 305 of FIG. 3B. The floating-point multiplier 305 consists of a [[reduced-precision]] multiplier 330 followed by a variable shift unit 335. The floating-point multiplier 305 is demonstrated with a 3-bit multiplier. To further simplify the full multiplication circuit 301 of FIG. 3A, the quantization levels may be restricted to powers of two. Multiplications with these values can be realized with bit shifts as illustrated in a variable shift [[multiplier]] unit 350 of FIG. 3C."

Please amend the paragraph beginning at page 7, lines 9-23 as follows:

The complexity of the multiplier implementations 301, 305~~, and 350~~ may be quoted in equivalent NAND gates while performance can be indicated with the maximum signal-to-noise ratio of two types of signal encoded with the respective quantization levels. The first signal can be a triangular wave, which exhibits a

constant density between the maximum and minimum values. The second signal can be a raised cosine signal that is more representative of the densities of windows. The full multiplier 301 has a complexity or "number of gates" of 1381 that directly influences its cost. Further, the full multiplier 301 [[it]] has 4096 quantization levels, a triangle wave signal-to-noise (SNR) ratio of 78.3 dB, and a raised cosine SNR ratio of 78.8 dB. The variable shift [[multiplier]] <u>unit</u> 350 as illustrated and has a complexity of 113 gates, 8 quantization levels, a triangle wave SNR of 14.5 dB and a raised cosine SNR of 16.2 dB. Additional embodiments of the invention may incorporate additional methods to quantize one of the operand, and implement a multiplier. In one embodiment of the invention, a memory device may be used in place of the multiplier, where all possible outcomes of the multiplier may be stored and retrieved."

Please amend the paragraph beginning at page 7, lines 24-30 as follows:

"Noise shaping, a technique known in the art, allows the design of apodization capable receive and transmit channels, such as those previously illustrated in 210 of FIG. 2[[.]], without multipliers 260. A beamforming circuit with noise shaped apodization achieves much better performance than without apodization. For one embodiment of the invention the noise shaping technique, also labeled delta-sigma ($\Delta\Sigma$) modulation, can involve the conversion of a signal into a quantized format where a quantization error can be purposely colored <u>as would be appreciated by those having ordinary skill in the art</u>."

Please amend the paragraph beginning at page 8, lines 1-17 as follows:

"Illustrated in FIG. 4 is a method of operation required to encode a finite length signal 400 as required for one embodiment of the invention. The embodiment may require a window 410 to be passed through a $\Delta\Sigma$ modulator 430 to be encoded on a small number of quantization levels 435. However, because of transients caused by the internal state of $\Delta\Sigma$ modulators, they may realize a poor job of encoding finite length signals. Therefore, an additional embodiment of the invention may require the window ~~415~~ <u>410</u> to first be made periodic 420 by repeating it 425. Even then, the

output of the $\Delta\Sigma$ modulator ~~435~~ 430 will not be periodic because of the strongly nonlinear behavior of the quantizer. Taking a subset 440 to represent window ~~415~~ 410 may thus introduce distortion and increase in-band noise. A search process may be necessary to select a sequence that minimizes these effects. One alternative of the invention is to find the sequence with the smallest error power as would be appreciated by those having ordinary skill in the art. After it has been identified, it may be necessary to rearrange the order 445 of the selected subset if the first element does not correspond to the first one of the window. It is important to note that for one embodiment of the invention, the operations 400 need to be performed only once to produce a quantized window 450. Therefore, the operations 400 do not require any processing power during normal scanning operations."